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Enabling 8K displays - A story of 33M pixels, 2 CRTCs and no Tears!

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Ever seen a true 33 million pixel 8K display? The maximum display link bandwidth available with DisplayPort's highest bit rate of 8.1 Gbps/lane limits the resolution to 5K@60 over a single DP connector. Hence the only true 8K displays allowing upto full 60 frames per second are the tiled displays enabled using 2 DP connectors running at their highest bit rate across 2 CRTCs in the display graphics pipeline. Enabling tiled displays across dual CRTC dual connector configuration has always resulted in screen tearing artifacts due to synchronization issues between the two tiles and their vertical blanking interrupts.

Transcoder port synchronization is a new feature supported on Intel's Linux Graphics kernel driver for platforms starting Gen 11 that fixes the tearing issue on tiled displays. In this talk Manasi will explain how port synchronization is plumbed into the existing atomic KMS implementation. She will deep dive into the DRM and i915 code changes required to handle tiled atomic modesets through master and slave CRTCs lockstep mode operation to enable tearfree 8K display output across 2 CRTCs and 2 ports in the graphics pipeline. She will conclude by showing the 8K display results using Intel GPU Tools test suite.

Code of Conduct

Yes

GSoC, EVoC or Outreachy

No

Presenter: NAVARE, Manasi (Intel Corporation)

Session Classification: Main Track

Track Classification: Talk (half slot) (closed)