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… except that, in recent years, those defining a CPU architecture have also defined recommended methods for architecture binaries to interact with platforms (the “interface method”)

These interface methods are usually paired with a set of recommended platform operations to implement (“the operations”)
Why have standard CPU PM operations?

- **Portable binaries**
  - OS distributions
  - Emulators
  - Simulators
Why have standard CPU PM operations?

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  - OS distributions
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  - Simulators

- **Boot one kernel image on multiple vendor hardware platforms; push some platform variation behind the SBI**
What are some common interface methods?

- MMIO
- Special instructions (MSRs, coprocessor moves, etc.)
- Triggering an exception
- Jumps
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Almost nothing about these methods has any bearing on the power management operations themselves.
What’s important are the operations

The operations define the functionality
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The operations define the functionality

So what operations should be defined?
What’s important are the operations

The operations define the functionality

So what operations should be defined?

Start with stakeholders
Power management interface stakeholders
Power management interface stakeholders

- Anyone wanting binary portability across:
  - Different platform hardware
  - Hypervisors
  - Emulators
Power management interface stakeholders

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- Hardware power management engineers
Power management interface stakeholders

● Anyone wanting binary portability across:
  ○ Different platform hardware
  ○ Hypervisors
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● Hardware power management engineers

● Software power management engineers
Why define new PM operations?

So why not reuse PM operations from previous platform specifications?
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Learn (and borrow) from the past. Build something better!
An aside about RISC-V philosophy

“Big tent”

- The goal is to create recommendations and reference specifications, not mandatory requirements
An aside about RISC-V philosophy

“Big tent” approach

- The goal is to create recommendations and reference specifications, not mandatory requirements
- Example: if someone wants to take a 2010-era SoC with a MMIO platform interface and replace the proprietary CPU cores with RISC-V cores, we cannot (and do not wish to) compel the use of the RISC-V PM specification
An aside about RISC-V philosophy

“Big tent” approach

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- Example: if someone wishes to build a system with no platform firmware, that is fine too
So what should be defined?

- Some people think it should be very minimal
  - Hotplug and nothing more
So what should be defined?

- **Some people think it should be very minimal**
  - Hotplug and nothing more

- **Some people think it should be maximal**
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- Support querying the specific PM SBI features that are available
Starting points

- PM feature queries
- CPU hotplug
  - CPU hotplug & unplug
  - Query CPU hotplug state
- Platform reset/shutdown
- CPU idle
  - Maximum wakeup latency/Expected sleep residency
  - Explicit states?
- CPU suspend
- Thoughts?