Contribution ID: **144**   Type: **not specified**

Memory tiering

Monday, 12 September 2022 11:00 (30 minutes)

CXL enables exploration of a more diverse range of memory technology beyond the DDR supported by the CPU. Those memory technologies come with different performance characteristics from a latency & bandwidth point of view. This means the memory topology of platforms becomes even more complex.

There is a large burden on how to leverage tiered memory, from letting the end user control placement to trying to automatically place memory on behalf of the end user. This presentation intends to be a review of the choices and technology that are in development (memory monitoring, NUMA, …) and try to identify roadblocks.

I agree to abide by the anti-harassment policy

Yes

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Session Classification: Kernel Memory Management MC

Track Classification: LPC Microconference: Kernel Memory Management MC