Linux Plumbers Conference 2022

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Memory Tiering Jérôme Glisse / Google



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Agenda

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- Memory Pyramids
- NUMA Again
- Memory Tiering
- Discussion

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Memory Pyramids



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Memory Pyramids

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Register: 0.2 ns	Register: +∞
Cache: 1-40 ns	Cache: 200GB/s-3TB/s
HBM: 50-100ns	HBM: 256GB/s-2TB/s
Local CPU-DDR: 60-100ns	Local CPU-DDR: 50GB/s-200GB/s
Remote CPU-DDR: 120-200ns	Remote CPU-DDR: 50GB/s-200GB/s
CXL-DDR: 180-260ns	CXL-DDR: 60-120GB/s
NVM: 300-400ns	NVM: 4-60GB/s
Over network: 2-4µs	Over network: 10-80GB/s
Latency	Bandwidth

Register: KBytesCache: MbytesHBM: GBytesLocal CPU-DDR: TBytesRemote CPU-DDR: TBytesCXL-DDR: TBytesNVM: PBytesOver network: +∞

Capacity



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Capacity / Speed / TCO

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Capacity growth faster than memory performance

Physics⇒Capacity++⇒Power++

Memory large chunk of TCO (Power: 15W / DIMM ⇒ ~120W to 240W & upfront cost)



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Capacity & Bandwidth

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CPU core counts keep growing ⇒Bandwidth per cores barely improve ⇒Capacity per cores improve slower than needs

Density improvement coming to an end





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Same goal: keep improving compute performance

 \Rightarrow Hot data must be in the fastest memory

Through hardware == Like cache

Through software == Memory placement



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- Application can not access all its memory at the same time (not enough CPUs)
- Some data structure in an application are access more often than others
- Which data is access more often can change over application lifetime
- Some applications have predictable access pattern
- Others applications have random access pattern
 - Some applications can categorize its data into buckets:
 - From most frequently accessed to least frequently accessed



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Explicit vs Implicit

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Explicit placement:

Application place its data to most appropriate memory

Implicit placement: Kernel/Daemon place application memory

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NUMA Again



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NUMA Again

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Asymmetric bandwidth & latency⇒NUMA again

But even worse NUMA overlay on memory tiering





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NUMA lessons

Source 2022 Northead Action Conference 2022 Northead Action Co

Few application are NUMA aware Large application often are Smaller application can be through library (memory allocation)

⇒Mechanism like autoNUMA

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Memory Tiering



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Cold Page: a page that was not access in last N ms

Hot Page: access more than K times in last L ms

Threshold (N,K,L) can vary over time





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Measuring Success

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What metric can we use to measure success?

% of memory access to fastest memory for a thread ⇒More access to fast memory→Better perf

Not a silver bullet Applications with background activity dominating memory access



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Kernel Components

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Cold Pages detection

Hot Pages detection

Page Migration

Policy & Management

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Discussion



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Cold Page Detection

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• LRU, MGLRU

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- Good candidates⇒migrate before reclaim
- Access Bit
 - Clear Access Bit⇒No access over N ms
- DAMON





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DAMON == Data MONitor access

Is DAMON good enough ? Better to have cold page monitoring != hot page Cold page do not need region Region can hide cold pages



Hot Page Detection

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Hot Page

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- \Rightarrow Many access over short periods of time
- ⇒ Software monitoring need high frequency sampling
- ⇒ Large overhead to do software sampling

We want hardware for hot page detection

- Heatmap
- N most recently used address



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Existing kernel API good enough ?

move_pages() migrate pages() Do we want a more asynchronous API?

Something like io_uring but for memory ? Memory Migration

- Memory reclaim
 Virtual Address Space manipulation



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Policy & Management

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- Policy & Management:
- In kernel ? Like LRU
 - One solution fits all ?
- In userspace ?
 - Different strategy per application groups

memcg point toward userspace being a better places



Configuration

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How do we want to configure memory tiers ?

sysfs API

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Disconnect from NUMA distance

Can help bridge kernel & userspace management

See RFC: Memory Tiering Kernel Interfaces (v4)