

# Linux Plumbers Conference

Dublin, Ireland **September 12-14, 2022**

A decorative graphic of a green pipe network with various fittings, valves, and elbows, framing the central text.

## CXL Type-3 device discovery, configuration in firmware and prepare ACPI tables for kernel usage

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# Required ACPI tables for Kernel

## Memory Expansion:

- A Memory NUMA node describing System locality, resource affinity, hot plug capability. SRAT ACPI structure provides these boot time description for Processor and Memory Ranges.
- In addition, information regarding memory latency and bandwidth attributes between system localities help kernel manage resources more efficiently. HMAT ACPI structures helps in describing this information.

## CXL Root Device:

- A CXL aware Kernel needs presence of Root device in ACPI namespace for enumerating CXL devices present downstream, understanding properties related to interleaving across host bridges.
- An ACPI object with HID=ACPI0017 in firmware will allow kernel to know about the presence of CXL Root device . It also indicates presence of CEDT tables.
- An ACPI object with HID=ACPI0016 would make kernel aware of Host bridge presence and kernel can utilize it for enumeration and configuration of the same.



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# Required ACPI tables for Kernel

CEDT (CXL Early Discovery Table):

- Kernel CXL driver needs information about each CXL Host bridge present in system and also the memory window where software would map HPA to CXL device memory.
- ACPI object of type CEDT – CHBS would provide the pointer to CHBCR block and enabling kernel to program any necessary HDM decoder configuration.
- ACPI object of type CEDT – CFMWS would describe the HPA memory window which kernel drivers can map to CXL Device memory based on discovery.



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# Development Platform for CXL

## Hardware

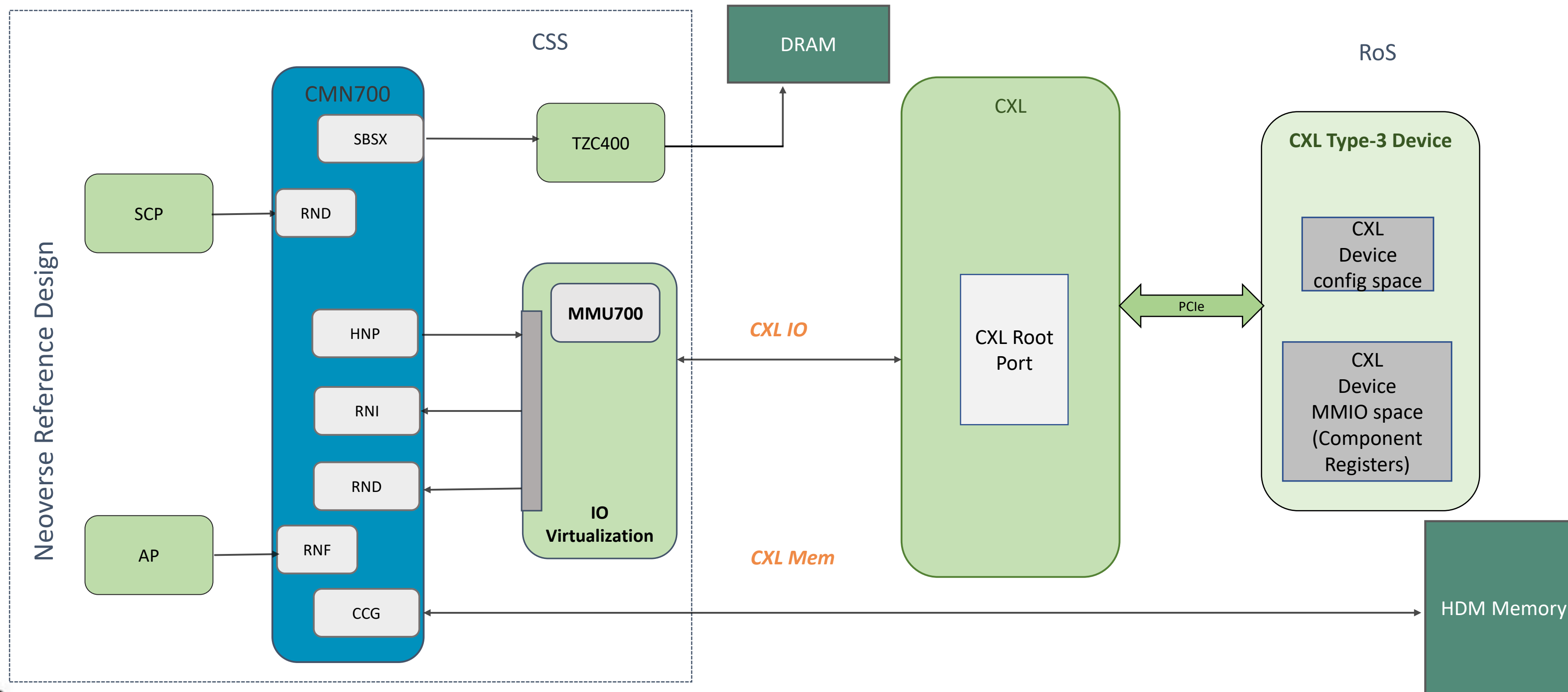
- Fixed Virtual Platform (FVP) is the test platform that are complete simulations of an Arm system, including processor, memory and peripherals.
- Neoverse RD-N2 FVP is one of the reference design platform.
- CXL 2.0 support continues to evolve on the RD-N2 FVP.
  - Supports DVSEC, Mailbox, CDAT, DOE
  - HDM (Interleaving support implementation is ongoing).



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# Development Platform for CXL



# Firmware Work

## System Control Processor (SCP) firmware

- Interconnect configuration , CXL device discovery.
- Find out device capabilities, DOE operations.
- Configure Interconnect based on device memory range.

## EDK2

- During Enumeration process discovers PCIe device with CXL and DOE capability.
- DOE operation, fetch CDAT(DSMAS, DSEMTS) tables. Find out supported Device memory range, type and associated attributes.
- Platform DXE prepares SRAT, HMAT tables based on remote CXL memory ranges discovered by CXL DXE.
- Prepare CEDT and CXL root device structures.
- <https://github.com/SayantaP-arm/edk2-platforms/tree/cxl-type-3>

## Kernel

- As of now, utilizing the well covered CXL framework present in Kernel.
- CXL device memory is used as separate NUMA node.
- <https://github.com/SayantaP-arm/edk2/tree/cxl>

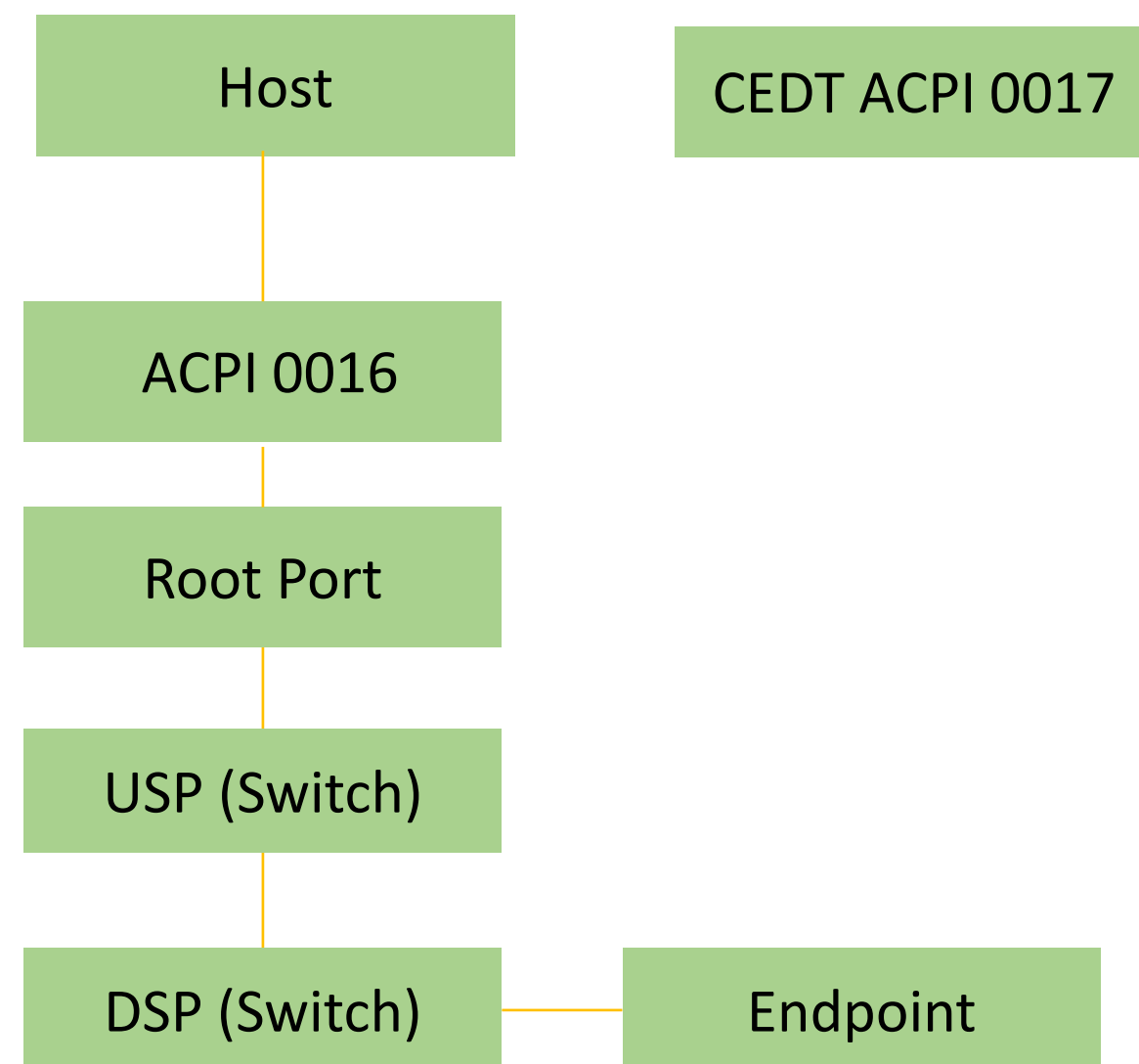


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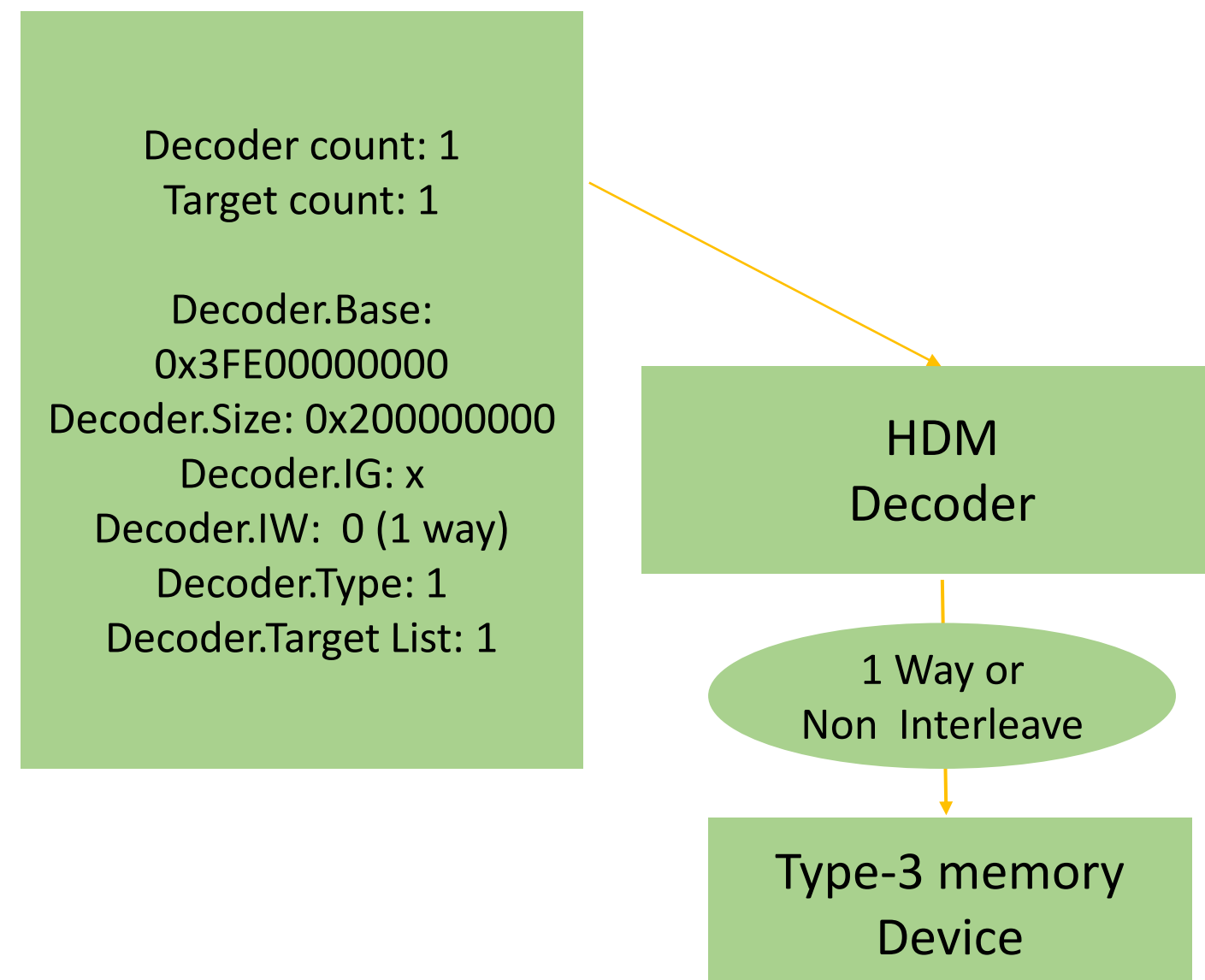
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# CXL with CEDT and Decoder Config

## CXL ACPI Hierarchy



## Decoder Configuration





# Status & Planned Tasks

## Completed

- Firmware development for discovering CXL device, mapping memory regions.
- DOE implementation in firmware for fetching CDAT structures. Prepare SRAT, HMAT tables to present CXL Type-3 memory as separate NUMA node in kernel.
- CEDT and other ACPI structures preparation and use of kernel CXL drivers for Host bridge non-interleaving HDM configuration.

## Ongoing and Future

- Development of interleaving capability in FVP and software.
- Continue engagement with CXL developer community and contribute to upstream CXL firmware and kernel support.
- Memory pooling is one of the next architectural work being investigated.
- SBRR coverage.
- Continue using upstream kernel for validating firmware work on the FVP platform.



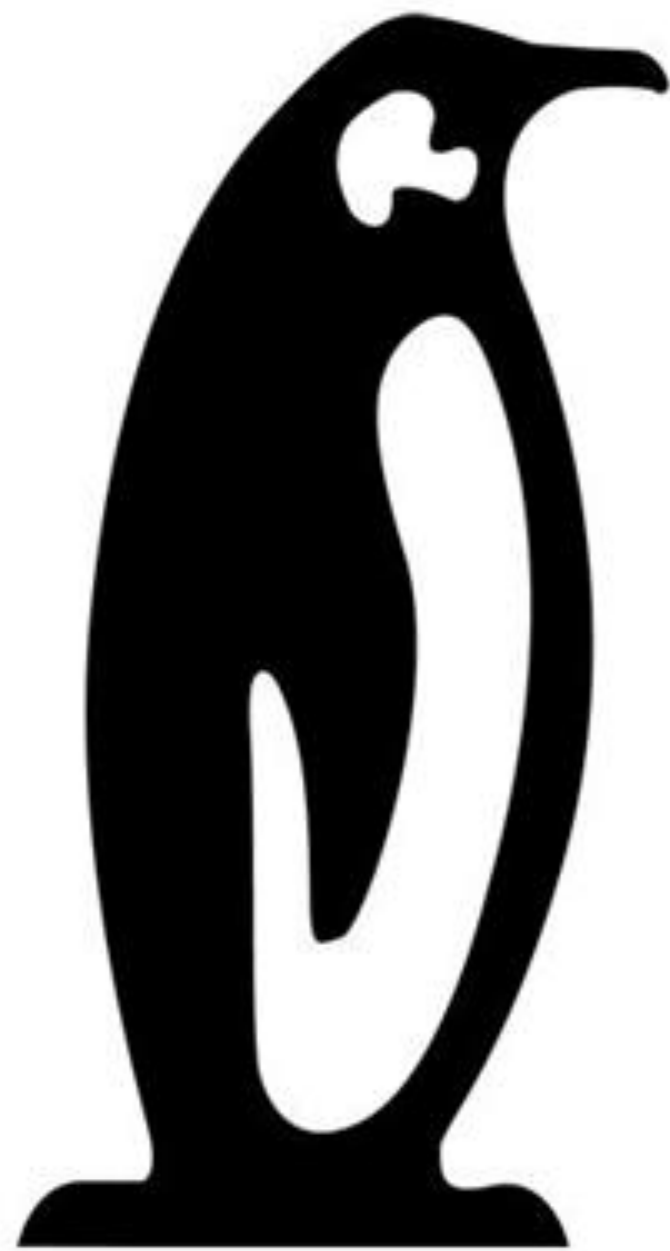
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## References

- Release gitlab link
  - [RD-N2 Cfg1 Platform Software guide](#)
- FVP download link
  - [Arm Ecosystem FVPs – Arm Developer](#)





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THANK YOU