

# Linux Plumbers Conference

Dublin, Ireland September 12-14, 2022

A decorative graphic of a green pipe network with various fittings, valves, and elbows, framing the central text.

# Libre Silicon in IoT

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QWERTY Embedded Design, LLC

September 14, 2022



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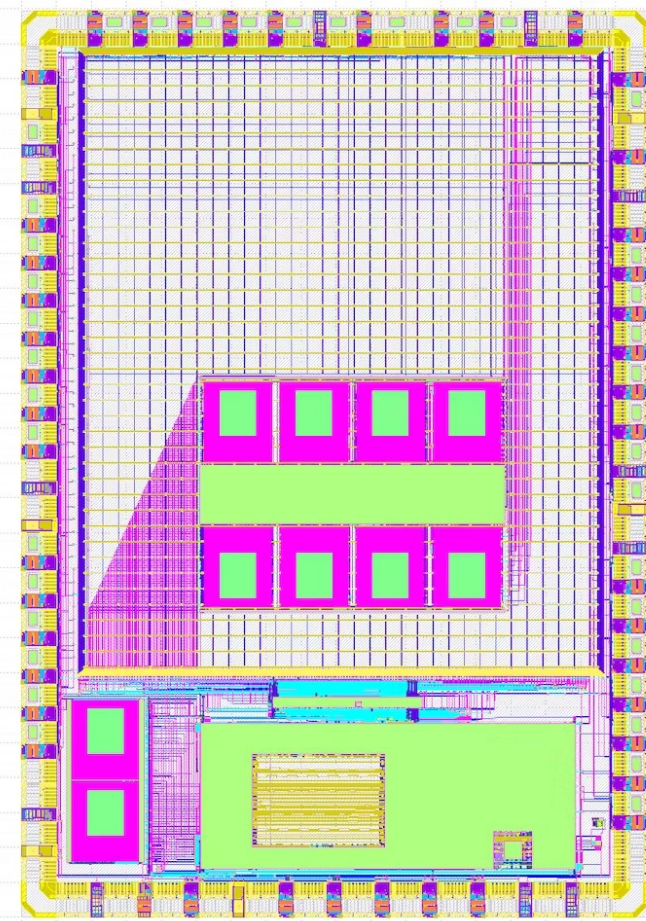
# Overview

## What is Libre Silicon?

- Why is Libre Silicon important?
- How is this possible?!
- Libre Silicon's role in IoT.

## PyFive

- Goals
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- Contributing



## ICE-V Wireless

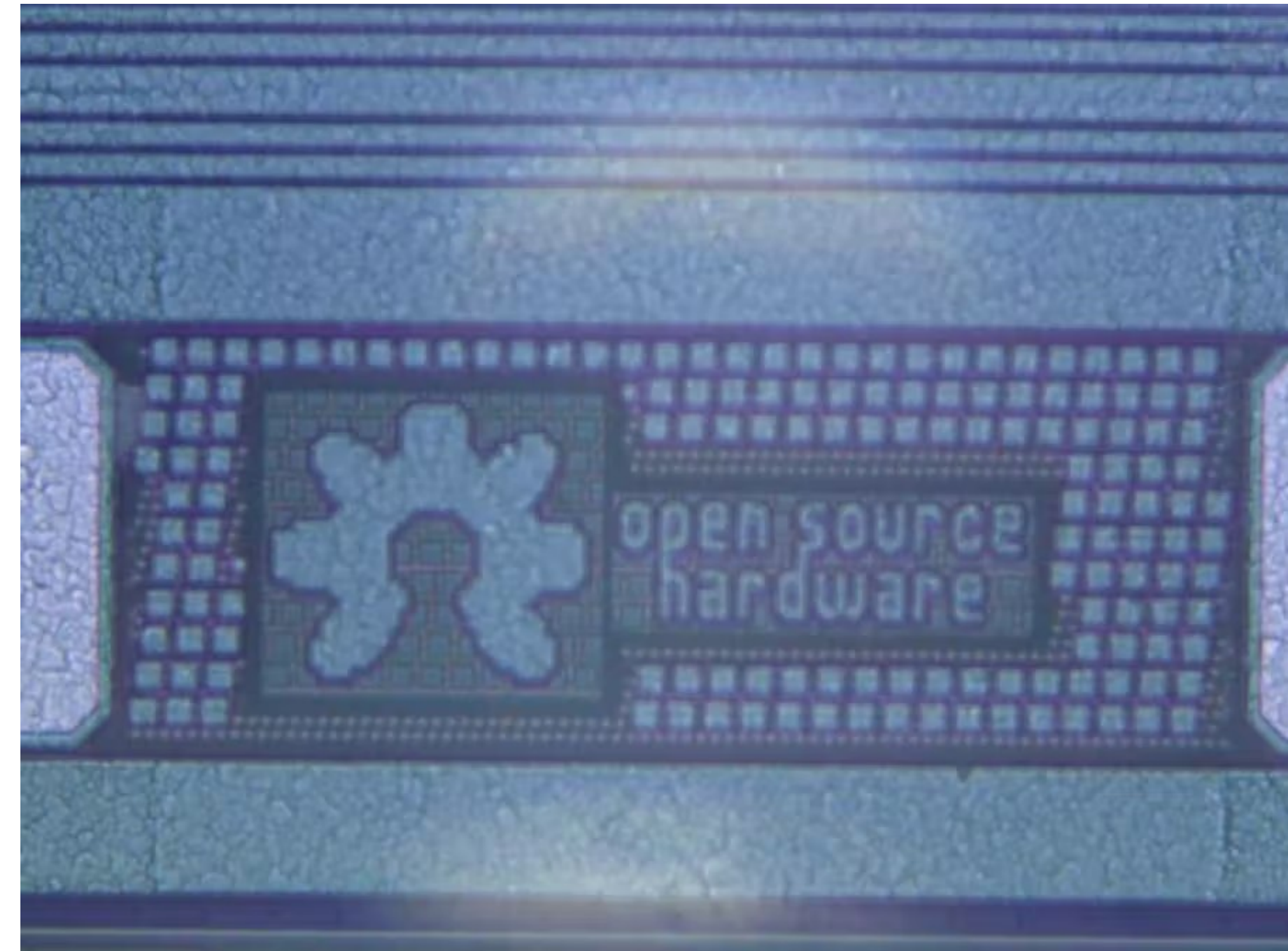
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# What is Libre Silicon?

Libre silicon represents the final form of open hardware, chips that are open source down to the mask level.

Meaning anyone with the design files could create new chips.



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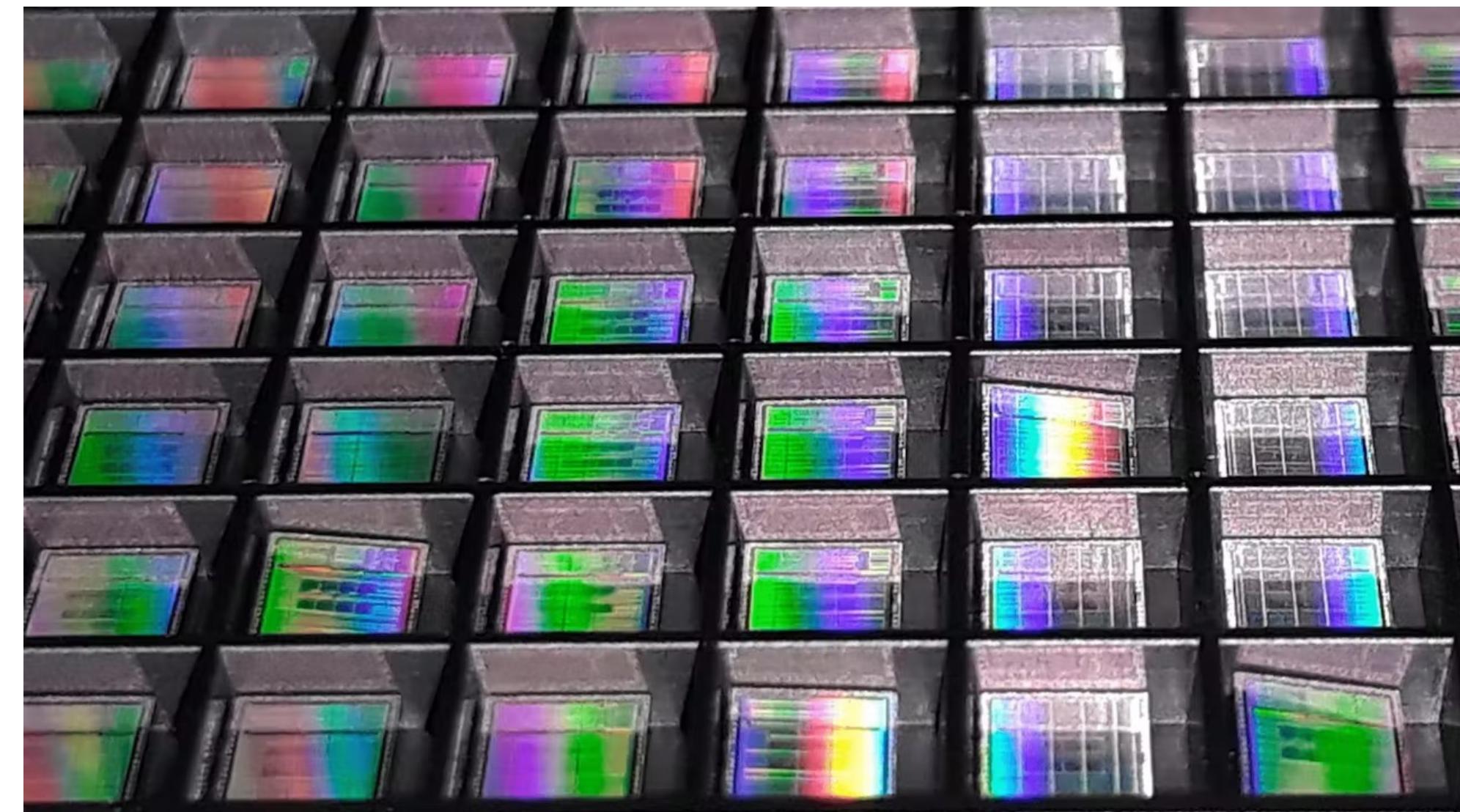
# What is Libre Silicon?

Why is Libre Silicon important?

- Design re-use
- Open collaboration
- Robust deeply inspectable design

<https://www.fossi-foundation.org/>

<https://wiki.f-si.org/>



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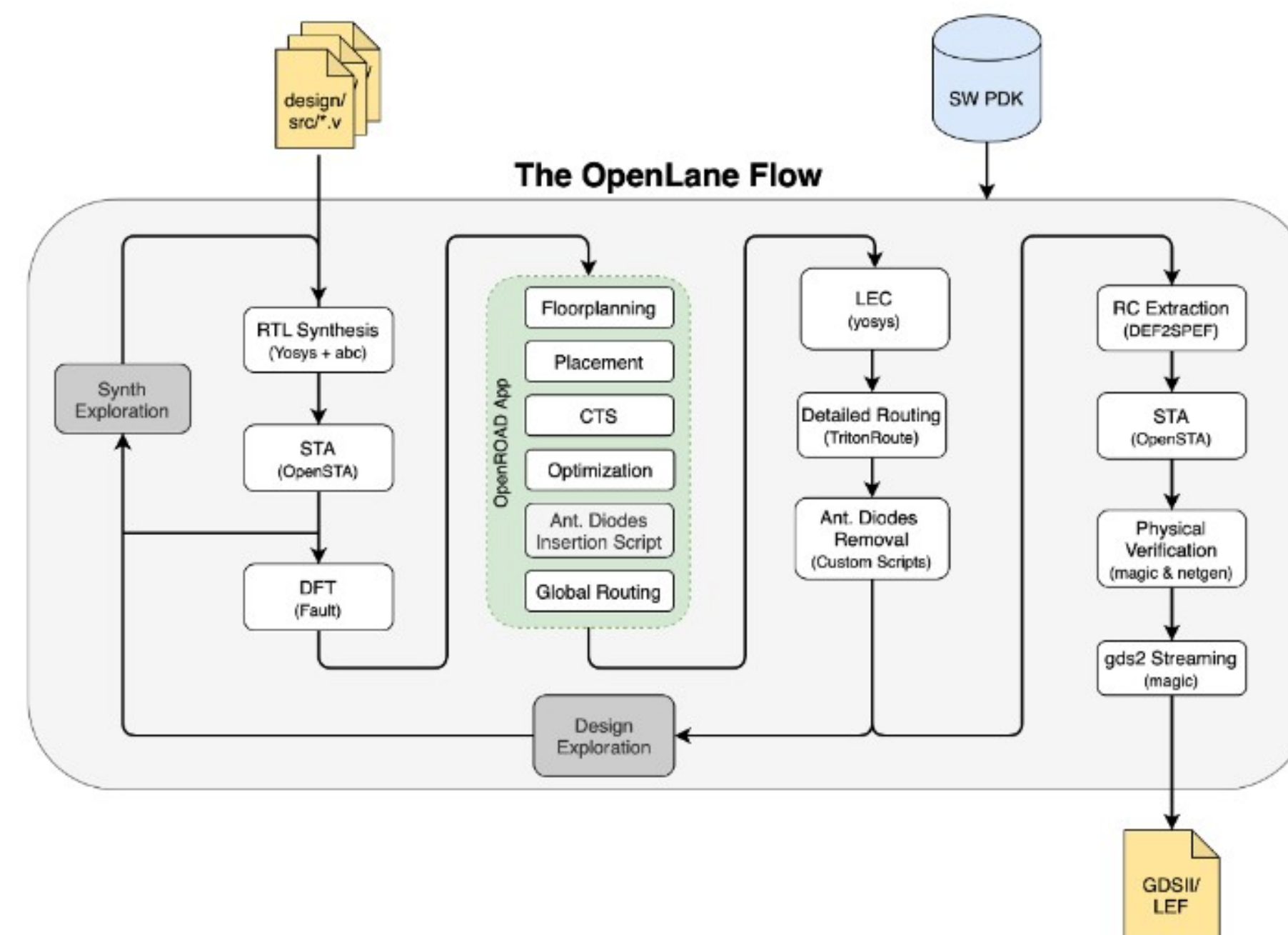
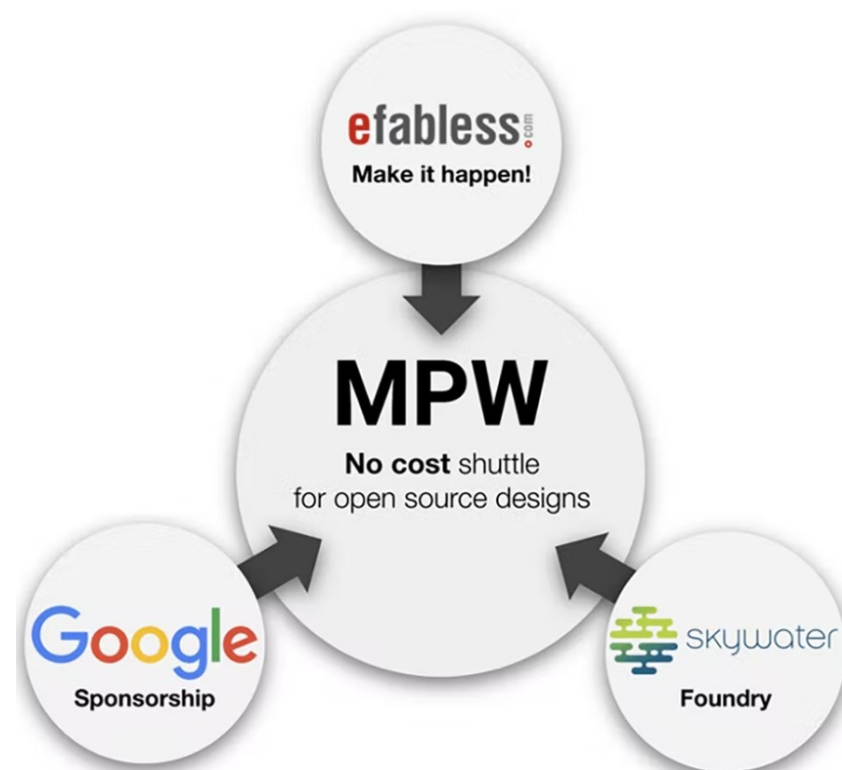
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# What is Libre Silicon?

How is this possible?!

Access to an open source PDK.  
Access to open source tools.  
Access to chip shuttles.

[https://efabless.com/open\\_shuttle\\_program](https://efabless.com/open_shuttle_program)  
<http://www.opencircuitdesign.com/magic/>  
<https://theopenroadproject.org/about-us/>  
<https://yosyshq.net/yosys/>  
<https://people.eecs.berkeley.edu/~alanmi/abc/>



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# What is Libre Silicon?

## Libre Silicon's role in IoT.

As trailing edge foundries begin to open up their PDKs, IoT solution developers are able to innovate and develop new IP with much lower initial cost.

Most IoT devices typically don't need the latest chip technology and will be the one of first markets to benefit from these new open ecosystems.



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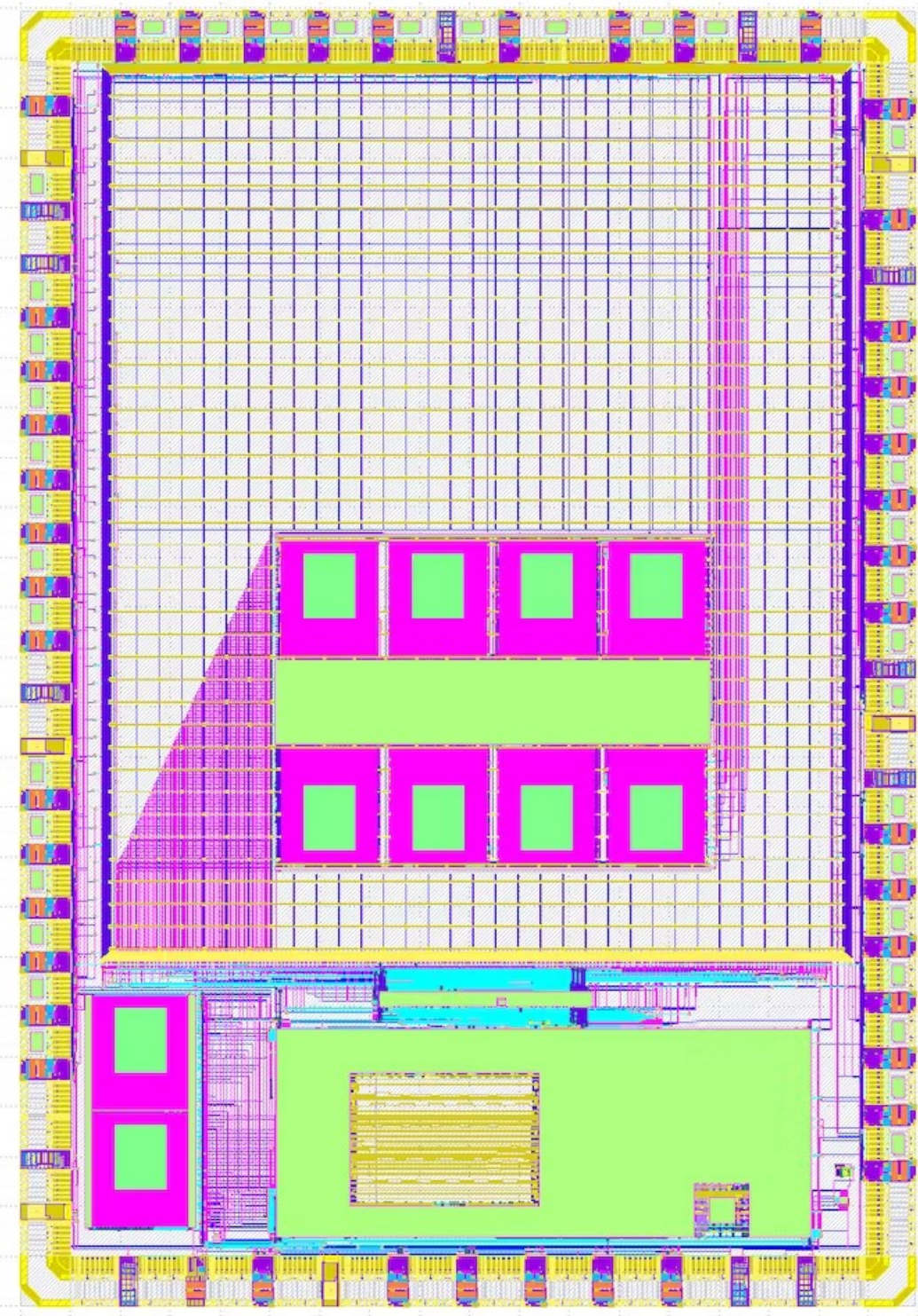
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# PyFive

## Goals

The goal of the PyFive project is to create a community driven RISC-V based MCU with the ability to easily support CircuitPython.

It would host a VexRiscV processor and have a USB interface along with other standard peripheral interfaces. Stretch goals included having an FPGA interface and/or software defined peripherals.



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<https://riscv.org/>

<https://github.com/SpinalHDL/VexRiscv>

<https://circuitpython.org/>



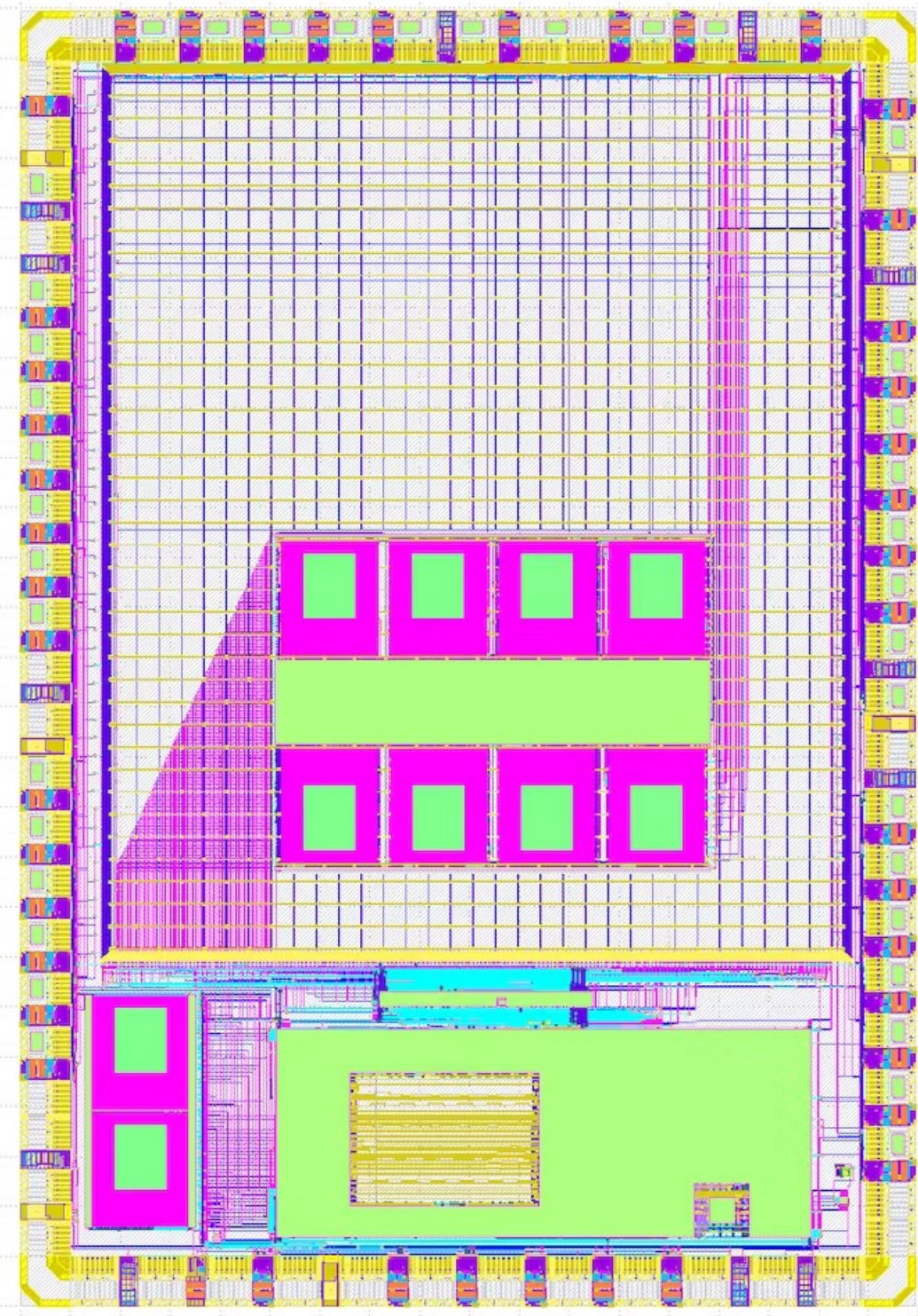
# PyFive

## Status

The PyFive ASIC was one of the 40 designs selected to be included on the first eFabless/Google/Skywater shuttle (MPW-1).

The first PyFive design was intended to be a test of the ASIC implementation of the no2usb USB core by Sylvain Munat (tnt).

The USB core was hardened along with some UART, video and PDM IP to fill in more of the available area on the chip design.



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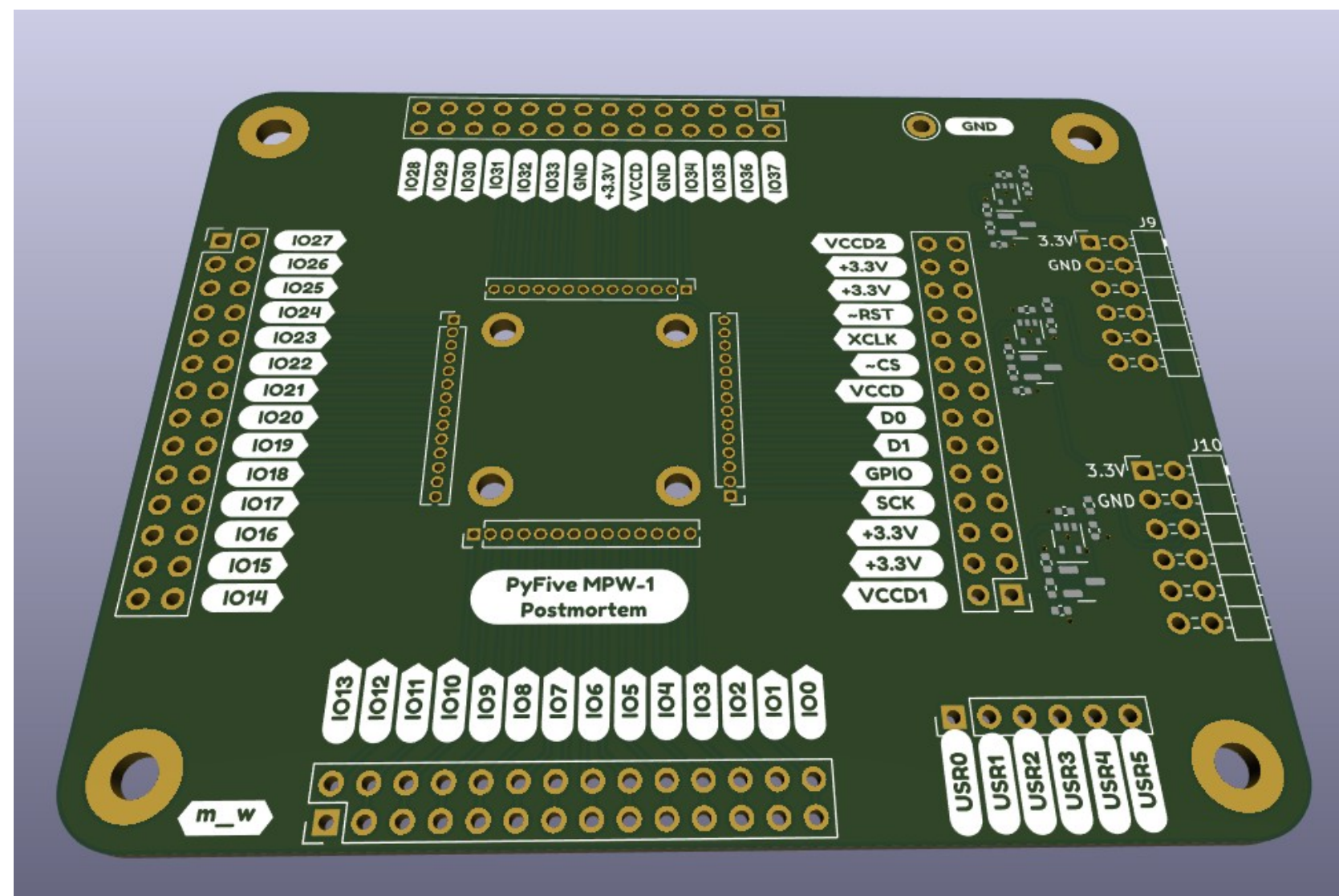
<https://github.com/PyFive-RISC-V>

<https://github.com/no2fpga/no2usb>

# PyFive

## Status

MPW-1 chips had hold time violations but tnt was able to get at least some life from the chips using a special post-mortem PCB design.



[https://www.youtube.com/watch?v=f\\_G5ad8SbHo](https://www.youtube.com/watch?v=f_G5ad8SbHo)



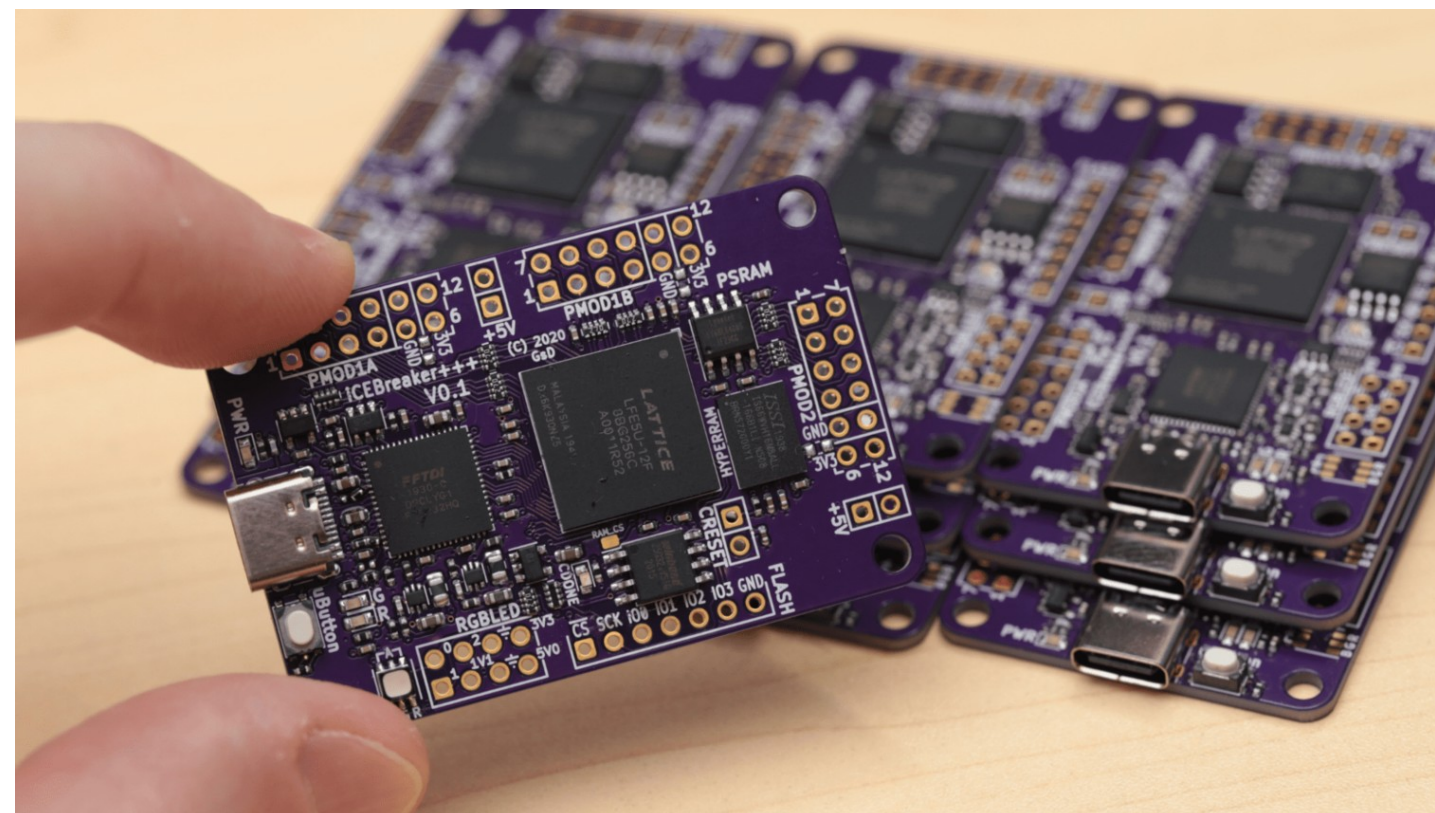
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# PyFive

## Status

While waiting for the first batch of chips to be delivered, the PyFive team further developed the IP and a firmware implementation of CircuitPython on a special ECP5 FPGA board designed by Greg Davill.



<https://github.com/gregdavill/advent-calendar-of-circuits-2020/tree/main/icebreaker%2B%2B-ram>  
<https://github.com/PyFive-RISC-V/circuitpython>



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# PyFive

## Contributing

The project is openly developed on Github and the QWERTY Embedded discord sever. People that are wanting to get involved can join the discussion there.

There is a GroupFund campaign to allow the community and corporate sponsors help fund development.

For those interested in the Caravel shuttle and surrounding ecosystem there is a slack channel.

<https://discord.gg/N5Xe3eBdzb>

<https://groupgets.com/campaigns/1038-pyfive-asic>

<http://join.skywater.tools/>

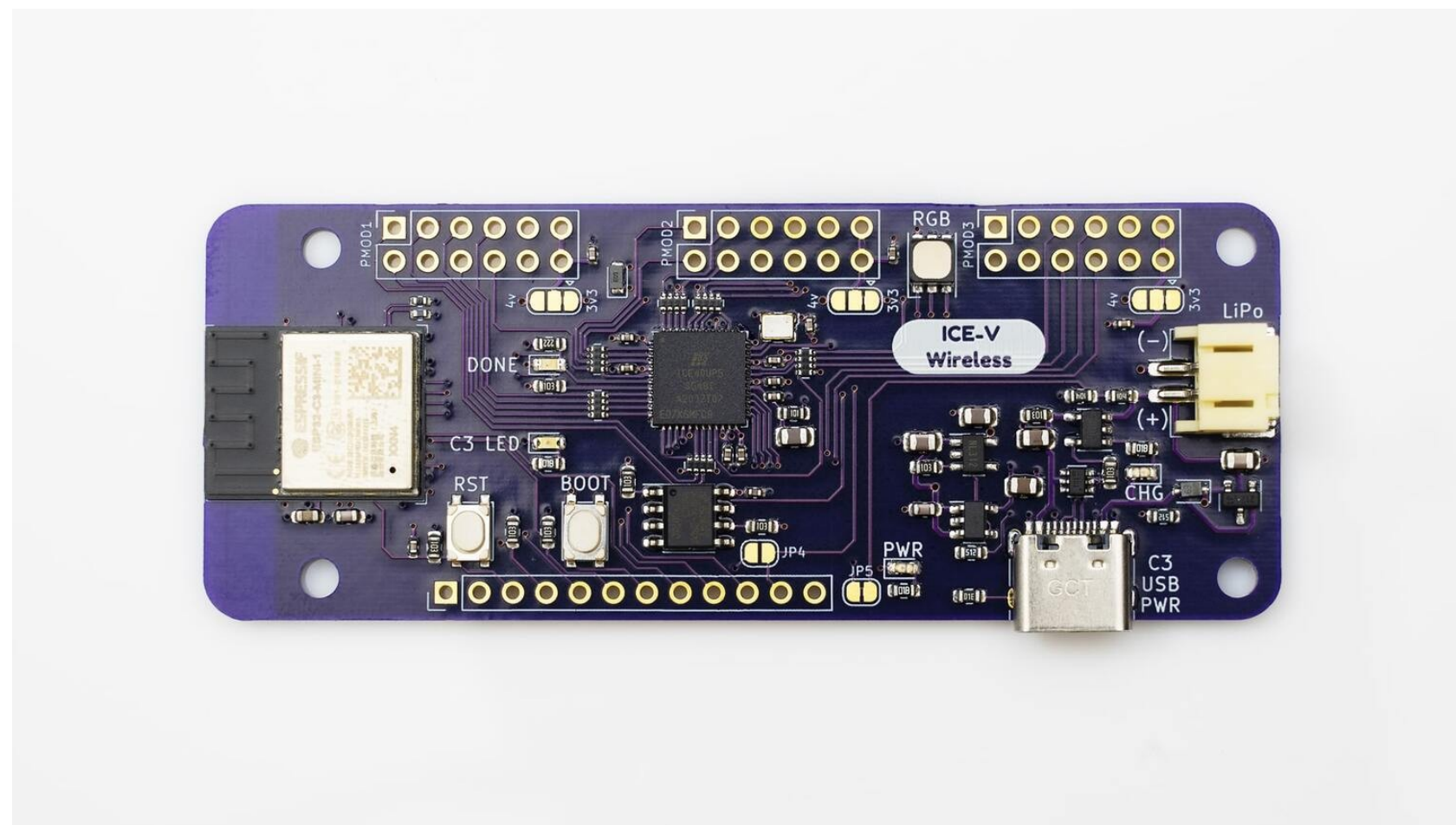


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# ICE-V Wireless

## About



ICE-V Wireless is a development board, allowing Wi-Fi and Bluetooth control of an FPGA by combining an Espressif ESP32-C3 and a Lattice iCE40 FPGA.

Allows for quick development with the Espressif IDF and YosysHQ open source FPGA toolchain.

The hardware was designed in KiCAD and is fully open source.

<https://docs.espressif.com/projects/esp-idf/en/latest/esp32/get-started/>  
<https://github.com/YosysHQ/oss-cad-suite-build>



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# ICE-V Wireless

## Status

**ICE-V Wireless**  
ICE40UP5K FPGA module with wireless interface driven by ESP32-C3.

**Funded**



**101% Funded**

★ 100 Goal

✓ 101 of 100 Backed

! 149 of 250 units are still available

\$75.00 + Shipping

Twitter, GitHub, Facebook, LinkedIn, Email, Share

FAQ ?

1 of 3



The ICE-V was successfully crowd funded on GroupGets and will be shipping to backers soon.

<https://groupgets.com/campaigns/1036-ice-v-wireless>

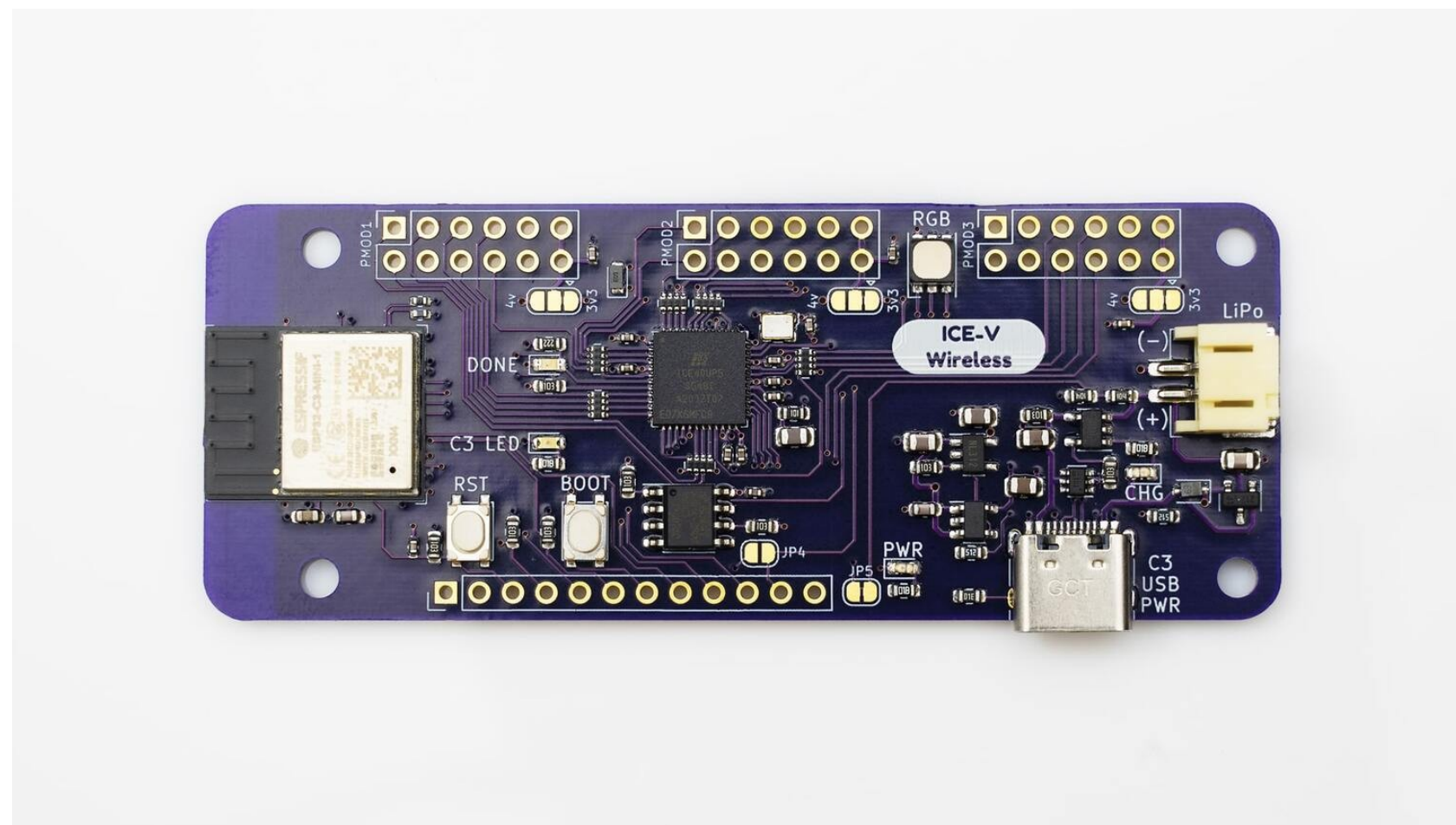


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# ICE-V Wireless

## Contributing



Efforts are coordinated through Github, Discord, and Twitter.

<https://github.com/ICE-V-Wireless>

<https://discord.gg/DM8xAN4Jjx>

<https://twitter.com/QwertyEmbedded>



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